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(54) Title: S-SHAPED CERAMIC FEEDTHROUGH

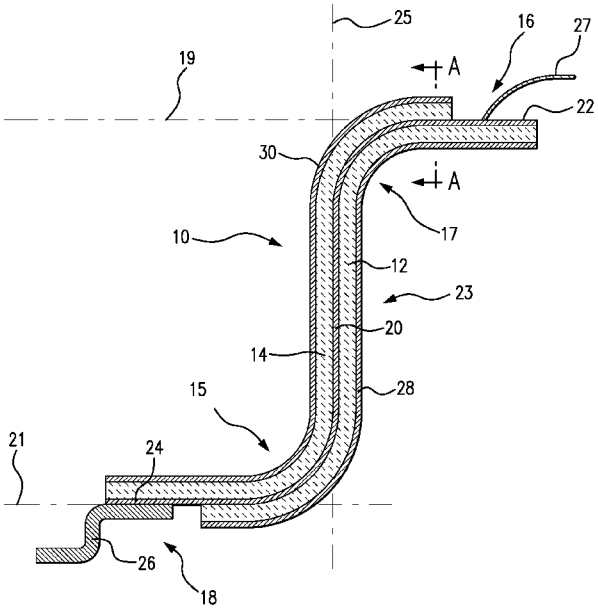

FIG. 3

(57) Abstract: An electrical interconnect 10 has a non-planar ceramic substrate 12, 14 with opposing first 10 and second 18 ends. A first conductive layer 20 having first 22 and second 24 opposing sides is disposed within the ceramic substrate 12, 14 with one of the first 22 and second 24 opposing sides exposed at the first end 16 and one of the first 22 and second 24 opposing sides exposed at the second end 18. The electrical interconnect 10 is useful to join an integrated circuit in a hybrid package to a circuit board in high frequency communication applications.

WO 2016/003587 A1

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S-SHAPED CERAMIC FEEDTHROUGH

[0001] The disclosure relates to a ceramic feedthrough for use in a high frequency signal transmission device. More particularly, a stripline transmission line is surrounded by a ceramic portion. This ceramic portion is then covered with a ground metallization.

[0002] High frequency electronic packages are frequently hybrid packages containing a multiple devices. The hybrid package is solder attached to a circuit board for use in high data rate communication systems. A number of requirements are imposed on an interconnect that joins the hybrid package to the circuit board. First, the interconnect must be capable of transitioning the electrical signal from the location of integrated circuits inside the housing of the hybrid package to lower levels that make contact with the circuit board. The signal path from the integrated circuits to the circuit board must simultaneously provide good signal integrity, solderable connection to the circuit board and transverse the requisite distance.

[0003] Second, the hybrid packages require electrical interconnects with performance that is effective over a very wide frequency bandwidth, nominally from 0 to 50 GHz or even 80 GHz. This wide band performance is required to maintain signal integrity of the information carried along the electrical interconnects. If the signal integrity is not maintained, then the information carried along the electrical interconnects will become unusable and the information could be lost.

[0004] Third, the interconnects must be compatible with the solder used to attach to circuit boards using standard surface mount methods. Solder attach is important because it offers the board level system integrator flexibility in processes and a capability to use low cost manufacturing processes.

[0005] To demonstrate the importance of signal integrity, consider the effect of poorly performing interconnects. The effect may be illustrated by eye performance results from the signal passing through the electrical interconnect. In telecommunications, an eye diagram is an oscilloscope display that shows a digital data signal that is repetitively sampled. It is called an eye diagram because, for several types of coding, the pattern looks like a series of eyes between a pair of rails. It is an empirical method used for the evaluation of combined effects. It is commonly used for high speed communication signals as an indication of the quality of the signal. For interconnects, the eye diagram shows undesired effects within the interconnects that will degrade the signal performance.

[0006] Several signal performance measures can be derived by analyzing the eye diagram. If the signals are too long, too short, poorly synchronized with the system clock, too high, too low, too noisy, too slow to change, or have too much undershoot or overshoot, this can be observed from an eye diagram. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to intersymbol interference and noise appears as closure of the eye pattern. An exemplary eye diagram with good performance is illustrated in Fig. 1. The eye 2 has symmetry and is uniform in shape.

[0007] The eye diagram illustrated in Fig. 2 shows the effect of transmission line dispersion, an electrical interconnect effect that degrades eye performance. Dispersion causes the transmission line propagation constant to be non-linear with frequency and line impedance to change as a function of frequency. The eye 4 lacks symmetry and is not uniform in shape. Other effects that degrade eye diagram performance include a stray inductive or capacitive parasitic as part of the electrical interconnect.

[0008] One prior high speed interconnect is a metal box with high quality coaxial connectors. The connectors are approximately 12.7 mm x 12.7 mm x 6.35 mm (0.5 inch x 0.5 inch x 0.25 inch) and require coaxial cable for connection. While these connections are capable of providing high quality interconnect performance over a very broad frequency range, they are not surface mountable. The connectors are too large to effectively integrate with a compact telecommunications equipment box.

[0009] A high speed interconnect is disclosed in United States Patent No. 8,933,450, titled "High-Frequency Transmitting Device," by Okumichi et al. Figures 1A - ID of US 8,933,450 illustrate a microstrip or coplanar waveguide transmission line forming a vertical transition from a top layer to a bottom layer. This approach utilizes a coaxial section that allows transition of the electrical signal from a layer with integrated circuits down to a layer that contacts with a circuit board. The coaxial section is formed using a center conductor via and a series of vias that form an electrical ground contact. This permits the signal to travel over transmission lines that are matched or nearly matched to the required system impedance, that is normally 50 ohms. A drawback with this approach is that it requires the electrical system to make an abrupt 90° bend in at least two locations which degrades electrical performance. The 90° bends occur at transition points at the top and at the bottom of the ceramic stack. One attempt at addressing this drawback is to use a stair-stepped via structure as mentioned in US 8,933,450. This

approach adds additional transition discontinuities which must be compensated and degrade electrical performance. Another drawback is that it requires a transition from co-planar waveguide (CPW), or microstrip, transmission line to coaxial transmission at two locations. This transition further degrades the electrical performance because the electric field distributions are so different between horizontal CPW or microstrip and the vertical coaxial line.

[0010] An electrical interconnect has a non-planar ceramic substrate with opposing first and second ends. A first conductive layer having first and second opposing sides is disposed within the ceramic substrate with one of the first and second opposing sides exposed at the first end and one of the first and second opposing sides exposed at the second end. The electrical interconnect is useful to join an integrated circuit in a hybrid package to a circuit board in high frequency communication applications.

[0011] FIG. 1 is an eye diagram illustrating good performance by an electrical interconnect.

[0012] FIG. 2 is an eye diagram illustrating poor performance by an electrical interconnect.

[0013] FIG. 3 is a cross-sectional view of an S-shaped ceramic feedthrough as disclosed herein.

[0014] FIG. 4 is a sectional view of a first embodiment of the S-shaped ceramic feedthrough of Fig. 3.

[0015] FIG. 5 is a sectional view of a second embodiment of the S-shaped ceramic feedthrough of Fig. 3.

[0016] FIG. 6 is a sectional view of a third embodiment of the S-shaped ceramic feedthrough of Fig. 3.

[0017] FIG. 7 schematically illustrates coupled transmission lines for use with a first amplifier circuit.

[0018] FIG. 8 schematically illustrates coupled transmission lines for use with a second amplifier circuit.

[0019] FIG. 9 shows a first process step used for the manufacture of the S-shaped ceramic feedthrough of Fig. 3.

[0020] FIG. 10 shows a second process step used for the manufacture of the S-shaped ceramic feedthrough of Fig. 3.

[0021] FIG. 11 shows a third process step used for the manufacture of the S-shaped ceramic feedthrough of Fig. 3.

[0022] Like reference numbers and designations in the various drawings indicated like elements.

DETAILED DESCRIPTION

[0023] An electrical interconnect with the exemplary shape of an S-shaped ceramic feedthrough 10 is illustrated in cross-sectional representation in Fig. 3. The S-shaped ceramic feedthrough 10 has a non-planar ceramic substrate portion that provides structural support. This ceramic portion includes a first layer 12 and a second layer 14 fused together as described hereinbelow. The fused first layer 12 and second layer 14 are S-shaped, with a first radius of curvature 15 about equal to a second radius of curvature 17, to smoothly transition an electrical signal from a package connect portion 16 to a board connect portion 18. Disposed between the first layer 12 and the second layer 14 is an electrically conductive stripline 20. A first microstrip 22 extends from stripline 20 and is supported by the package connect portion 16 of the first layer 12 and is for electrical interconnection to integrated circuits contained in a hybrid package, such as by wire bonding 27. An opposing second microstrip 24 extends from stripline 20 and is supported by the board connect portion 18 of the second layer 14 and is for electrical interconnection to a circuit board or similar structure. The first microstrip 22 and the second microstrip 24 are essentially co-planar as indicated by projection lines 19, 21 and approximately perpendicular to mid-portion 23 as indicated by projection line 25. A metallic lead 26 or a solder ball (not shown) may facilitate electrical interconnection between the second microstrip 24 and the circuit board. A ground metallization 28, 30 coats exterior surfaces of the fused first layer 12 and second layer 14 of the ceramic section.

[0024] The first microstrip 22 is supported by the first layer 12 of the ceramic portion. This provides a rigid surface for wirebonding to integrated circuits within the hybrid package housing. The ground metallization 28, 30 provides isolation to minimize electrical signal radiation to other circuits and provides a ground reference for the transmission lines. The ground metallization 28, 30 also provides a surface for brazing to the metal housing of the hybrid package which results in a hermetic seal. The shaped lead 26 at the second microstrip 24 of the S-shaped ceramic feedthrough 10 provides a solderable surface for connection to a circuit board and a stress relief between the ceramic-

based feedthrough 10 and, for example, a polymer-based printed circuit board. The first microstrip 22 is a matched transmission line with an electric field that is compatible with the stripline 20 and in the same plane, due to the smooth transition bend.

[0025] Particularly beneficial is the way that the high speed electrical path transitions from the microstrip level 22 to the circuit board connection point 24. The transition is implemented based on the use of a stripline transmission line. The transmission line is one continuous piece of stripline in ceramic that is formed, prior to final ceramic firing, into the shape required to transport the electrical signal. In this way, the transition avoids the use of vertical vias and abrupt signal transitions that are characteristic of some prior implementations.

[0026] The first microstrip 22 has a section of microstrip line that makes contact to integrated circuits. The second microstrip 24 has an attached lead 26 that makes contact between a circuit board and the S-shaped ceramic feedthrough 10. Disposed between the first microstrip 22 and the second microstrip 24 is a section of continuous stripline transmission line 20 that is formed into the required shape. Because cofired ceramic material is not rigid and is formable prior to final firing, the ceramic feedthrough can be bent into a desired shape to realize the transition. All of the transmission lines are optimized for 50 ohms, or other required system impedance, so that the electrical signal maintains high quality. The ceramic that surrounds the stripline transmission line section 20 is covered with ground metallization. With reference to Fig. 6, there may be vias 32 connecting the ground metallization 28 on the top side with the ground metallization 30 on the bottom side. The vias 32 contact the ground metallization 28, 30 that is on the top side and on the bottom side of the ceramic. The vias 32 are useful because they maintain electrical connection between the ground metallizations 28, 30 to avoid higher mode propagation.

[0027] The transmission stripline 20 within the S-shaped ceramic feedthrough may be multiple transmission lines or coupled transmission lines. Figs. 4 - 6 show the ceramic feed through in cross-sectional view along the reference line (A - A) in Fig. 3. Fig. 4 illustrates a single stripline 20. Fig. 5 illustrates two striplines 20, 20'. When there are multiple transmission lines, the vias 32 contacting the top metallization 28 and the bottom metallization 30 have the additional function of providing electrical signal isolation between the separate transmission striplines 20, 20'. Undesired coupling between circuits occurs when there is capacitive or inductive energy transfer and can have a detrimental

effect on signal integrity. At lower frequencies, coupling between transmission lines is treated as an effect that is linear with frequency and with the length of the line. At lower frequencies, this is a perfectly valid approach to within a few percent for many transmission lines. A more accurate approach is to approximate the coupled lines as a capacitance that is proportional to the length of the transmission lines. However, as frequency increases, the coupling between transmission lines can no longer be approximated by linear function or modeled with a simple capacitor, instead, they are modeled as coupled transmission lines. When the coupling is undesired, then the isolation vias 32 between the transmission striplines 20, 20' eliminates (or minimizes) the capacitive coupling between transmission lines. Although only two transmission striplines are shown in Fig. 5, it is possible for in excess of two transmission striplines to be within the same structure, either side by side or stacked within the ceramic.

[0028] An alternative, illustrated in Fig. 6, is coupled transmission striplines 20, 20'. Coupled transmission striplines are useful in certain applications that require coupled differential transmission lines to maintain signal integrity. There are many reasons that coupled transmission lines are used. One example is when the transmission striplines 20, 20' terminate into amplifiers 36 that require differential signals. One method to model the coupled striplines 20, 20' is to use even and odd mode impedances. The ceramic transition can be used to realize coupled transmission lines 20, 20' that are important for these types of circuits. With reference to Fig. 7:

$$Z_{even} = \infty$$

[0029] With reference to Fig. 8:

(1) even mode impedance matching

$$R_B = Z_{even}$$

(2) odd mode impedance matching

$$R_B \parallel R_A / 2 = Z_{0dd}$$

$$(Z_{even} \cdot R_A) / (2Z_{even} + R_A) = Z_{Qdd}$$

$$\therefore R_A = (2Z_{even} \cdot Z_{Qdd}) / (Z_{even} - Z_{Qdd})$$

[0030] FIG. 9 shows a first process step used for the manufacture of the S-shaped ceramic feedthrough. A first ceramic substrate 40 is a green compact of a ceramic material. A green compact means that the ceramic has been pressed together, but has not yet been fired. It is therefore flexible and may be formed without falling apart. A suitable ceramic is characterized by its ability to support the mechanical demands, ability to be

formed in the green (unfired) state, ability to be fired (sintered) into a homogeneous (or nearly homogeneous) piece, and its compatibility for high frequency electrical signal transport which includes appropriate dielectric constant. One suitable ceramic has a composition, by weight, of 90% - 95% aluminum oxide (High Temperature Cofired Ceramic technology). However, other glass and ceramic composition may be used *(i.e.* Low Temperature Cofired Ceramic technology). Conductive striplines 42 are placed on the first ceramic substrate. The number of striplines 42 and their spacing is dependent of the lead configuration of the finished feedthrough.

[0031] As a second process step, as shown in Fig. 10, A second ceramic substrate 44, also a green compact of the ceramic material is placed over the striplines 42 and pressed to abut the first ceramic substrate 40. The first 40 and second 44 ceramic substrates are sized and aligned to form the respective first microstrip 22 and second microstrip 24 (as seen in Fig. 3).

[0032] As a third process step, as shown in Fig. 11, the structure formed by the combination of the first ceramic substrate and the second ceramic substrate is placed in a mold and formed to a desired shape with transition 46 having appropriate curves at top and bottom and mid-portion of a desired length. Because the ceramic substrates are green compacts at this point, accurate control over curves and lengths is readily achieved. The structure is then fired to fused the ceramic components. A typical heat cycle for sintering a High Temperature Cofired Ceramic is heating to a temperature of from 1400°C to 1600°C for a time of from 30 minutes to 6 hours in a hydrogen-nitrogen (reducing) atmosphere or in a vacuum and then cooling to room temperature. A typical heat cycle for sintering a Low Temperature Cofired Ceramic is heating to a temperature of from 400°C to 850°C in an air (oxidizing) atmosphere or a time of from 10 minutes to one hour and then cooling back to room temperature. The fused structure is then sanded and polished along the direction of arrows 48 and then cut along lines 50 to complete the S-shaped ceramic feedthrough.

[0033] One or more embodiments of the present invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the ceramic piece may be bent upward from the package to form a transition that makes contact to a motherboard on the opposite side of the package. This approach is useful in cases where the thermal path of the electronics and the electronic signal path are on opposite sides of the package.

Another example is where the electrical signal will transition from one layer of the metal package to a separate signal layer within the package. In this modification to the invention, the transition allows high quality signal transmission within a metal package when the electronics inside the package are at different levels. Another modification is when the transition is used to transition to the external portion of the metal package, but rather than at the edge of the package, the transition can occur at an internal portion of the package allowing the external signal to exit the package without extending the package foot print. This approach may be useful in cases where a very compact package size is required.

WHAT IS CLAIMED IS:

1. An electrical interconnect 10, characterized by:
a non-planar ceramic substrate 12, 14 having opposing first 16 and second 18 ends; and
a first conductive layer 20 having first 22 and second 24 opposing sides disposed within the ceramic substrate 12,14 with one of said first 22 and second 24 opposing sides exposed at said first end 16 and one of said first 22 and second 24 opposing sides exposed at said second end 18.

2. The electrical interconnect 10 of claim 1 characterized in that said first end 16 and said second end 18 of said non-planar ceramic substrate 12, 14 are coplanar.

3. The electrical interconnect 10 of claim 2 characterized in that a mid-portion 23 of said non-planar ceramic substrate 12, 14 is approximately perpendicular to both said first end 16 and said second end 18.

4. The electrical interconnect 10 of claim 2 characterized in that opposing first and second surfaces of said non-planar ceramic substrate 12, 14 are coated with a conductive material 28, 30.

5. The electrical interconnect 10 of claim 4 characterized in that in addition to said first conductive layer 20, one or more additional conductive layers 28, 30, that are coplanar with said first conductive layer 20 are disposed within the ceramic substrate 12, 14 each of said one or more additional conductive layers 28, 30 also having one of a first and a second opposing sides exposed at said first end and one of said first and said second opposing sides exposed at said second end.

6. The electrical interconnect 10 of claim 5 characterized in that a plurality of electrically conductive vias 32 extend from said first conductive layer 28 to said second conductive layer 30 such that an electrical conductive via 32 extends along two opposing edges of each of said conductive layer 20 and said one of more additional conductive layers 28, 30.

7. The electrical interconnect 10 of claim 5 characterized in that a plurality of electrically conductive vias 32 extend from said first conductive layer 28 to said second conductive layer 30 such that an electrical conductive via 32 extends along one edge of said conductive layer 20 and one edge of one of said one of more additional conductive layers 20' with no electrically conductive via 32 disposed between said conductive layer 20 and an adjacent one of said one of more additional conductive layers 20'.

8. The electrical interconnect 10 of claim 5 characterized in that said first opposing side 16 of said first conductive layer 22 and said one or more additional conductive layers 28 is exposed at said first end of said ceramic conductor 12, 14 and said second opposing side 18 of said first conductive layer 22 and said one or more additional conductive layers 24 is exposed at said second end of said ceramic conductor 12, 14.

9. The electrical interconnect 10 of claim 8 characterized in that a wire bond 27 effective to electrically interconnect said electrical conductor 10 to an integrated circuit is bonded to said first opposing side 16 of said first conductive layer 22.

10. The electrical interconnect 10 of claim 8 characterized in that a conductive material 26 effective to electrically interconnect said electrical conductor 10 to a circuit board is bonded to said second opposing side 18 of said first conductive layer 22.

11. The electrical interconnect 10 of claim 9 characterized in that a conductive material 26 effective to electrically interconnect said electrical conductor 10 to a circuit board is bonded to said second opposing side 18 of said first conductive layer 22.

12. The electrical interconnect 10 of claim 11 characterized in that a radius of curvature 17 between said first end 16 and said mid-portion 23 of said non-planar ceramic substrate 12, 14 is about equal to a radius of curvature 15 between said mid-portion 23 and said second end 18 of said non-planar ceramic substrate 12, 14.

13. A process for the manufacture of an electrical interconnect 10, characterized by the steps of:

a). providing a first green ceramic compact 40 and disposing a plurality of electrically conductive strips 42 on said green ceramic compact 40, said plurality of electrically conductive strips 42 being parallel to each other and electrically isolated from each other;

b). placing a second green ceramic compact 44 on to a surface of said first green ceramic compact 40 with said plurality of electrically conductive strips 42 disposed therebetween with one of a first 22 opposing side of said plurality of electrically conductive strips 42 being supported by said first green ceramic compact40 and not covered by said second green ceramic compact 44 and a second 24 opposing side of said plurality of electrically conductive strips 42 being supported by said second green compact 44 and not covered by said first green compact 40;

c). shaping an assembly formed in step (b) to a desired shape; and

d). heating said assembly to a temperature and for a time effective to fuse said first green compact 40 to said second green compact 44.

14. The process of claim 14 characterized in that, prior to step (d), depositing a first metallic layer 28 on an exterior surface of said first green compact 40 and a second metallic layer 30 on an exterior surface of said second green compact 44.

15. The process of claim 14 characterized in that one or more electrically conductive vias 32 are formed to extend from said first metallic layer 28 to said second metallic layer 30.

16. The process of claim 14 characterized in that, in step (c), shaping said assembly such that said first opposing side of said plurality of electrically conductive strips 16 is coplanar with said second opposing side 18 of said plurality of electrically conductive strips 22, 24.

17. The process of claim 16 characterized in that, in step (c), shaping said assembly such that a mid-portion 23 of said plurality of electrically conductive strips 22, 24 is approximately perpendicular to said first opposing side 16 of said plurality of

electrically conductive strips which is coplanar with said second opposing side 18 of said plurality of electrically conductive strips 22, 24.

18. The process of claim 17 characterized in that, in step (c), shaping said assembly such that a radius of curvature 17 between said mid-portion 23 of said plurality of electrically conductive strips 22, 24 and said first opposing side 16 of said plurality of electrically conductive strips 22, 24 is approximately equal to a radius of curvature 15 between said mid-portion 23 of said electrically conductive strips 22, 24 and said second opposing side 18 of said plurality of electrically conductive strips 22, 24.

19. The process of claim 14 characterized in that said heating step includes heating to a temperature of between 1400°C and 1600°C for a time of between 30 minutes and 6 hours in a reducing atmosphere.

20. The process of claim 14 characterized in that said heating step includes heating to a temperature of between 400°C and 850°C for a time of between 10 minutes and one hour in an oxidizing atmosphere.

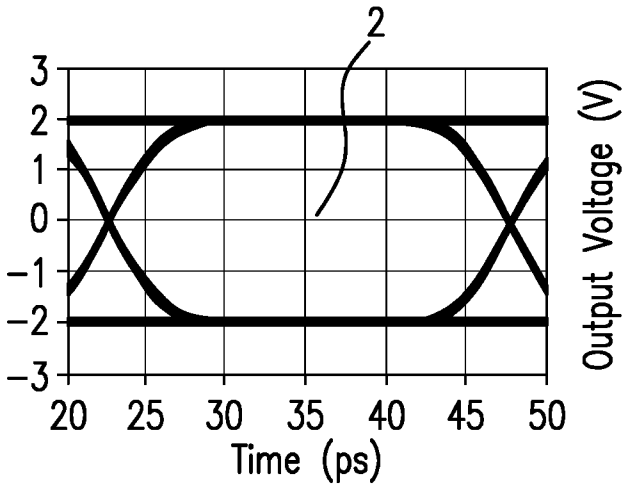

FIG. 1 PRIOR ART

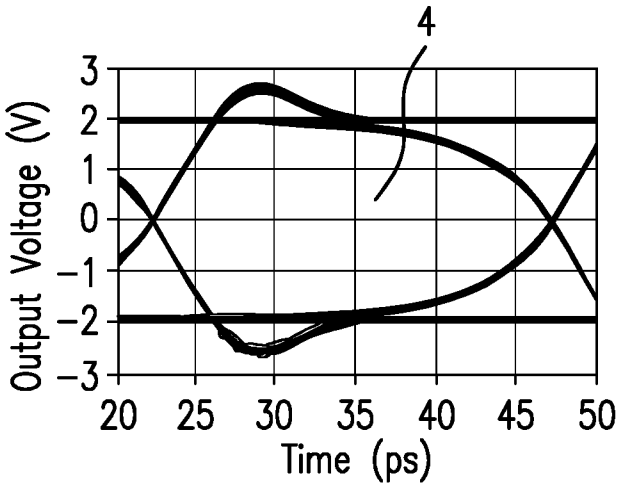

FIG. 2 PRIOR ART

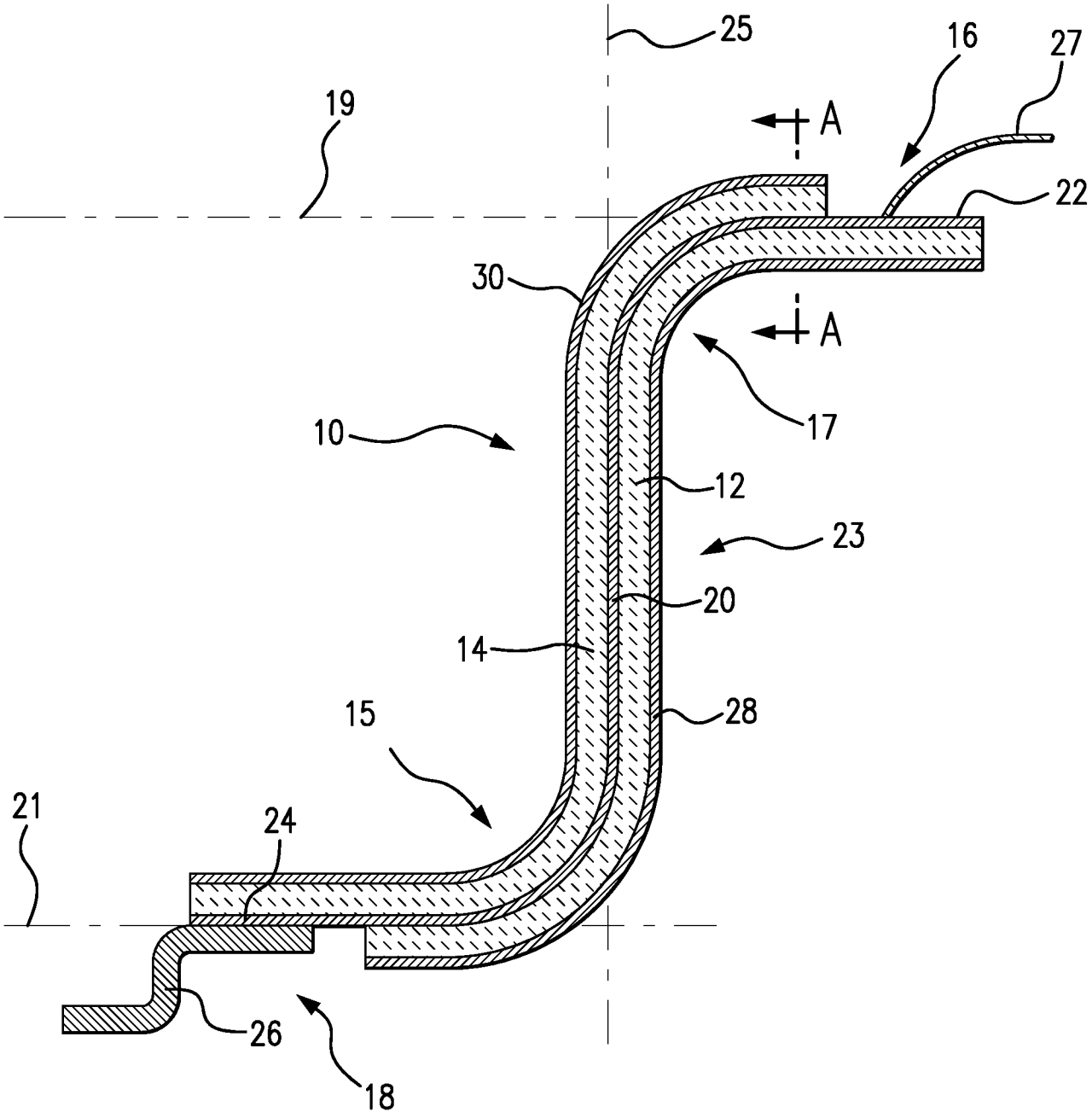

FIG. 3

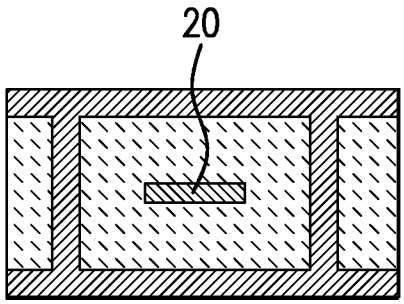

FIG. 4

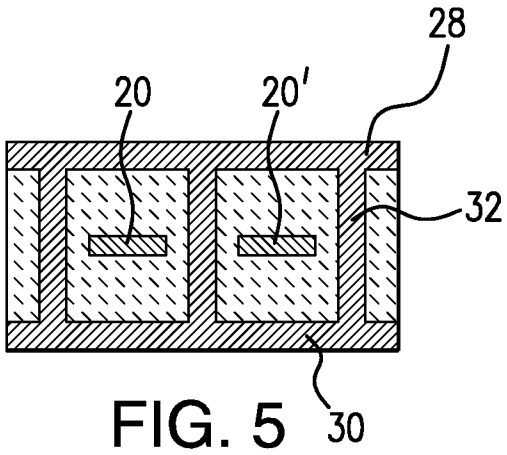

FIG. 5

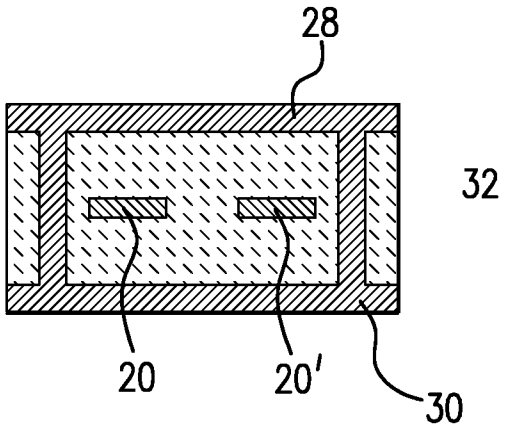

FIG. 6

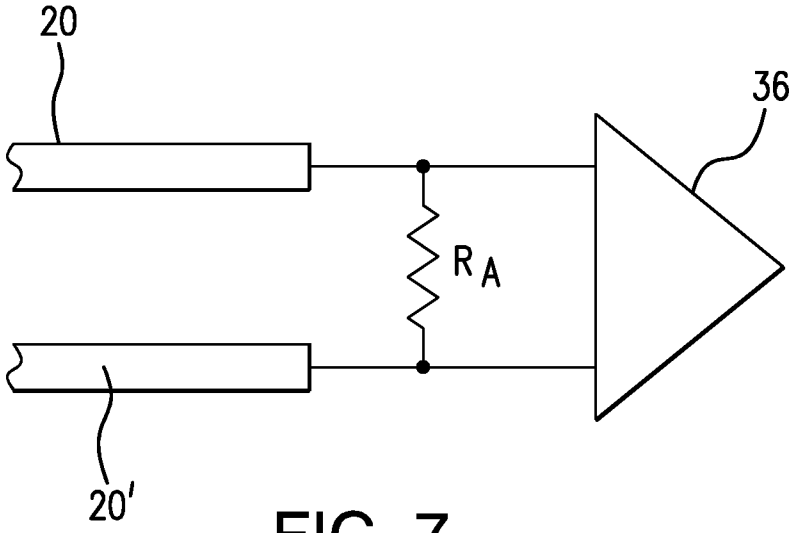

FIG. 7

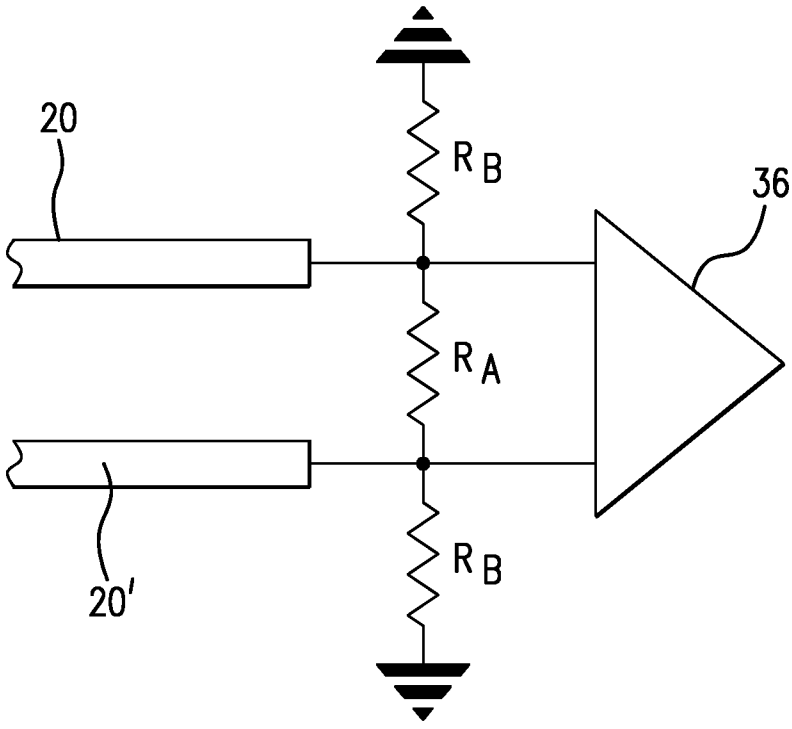

FIG. 8

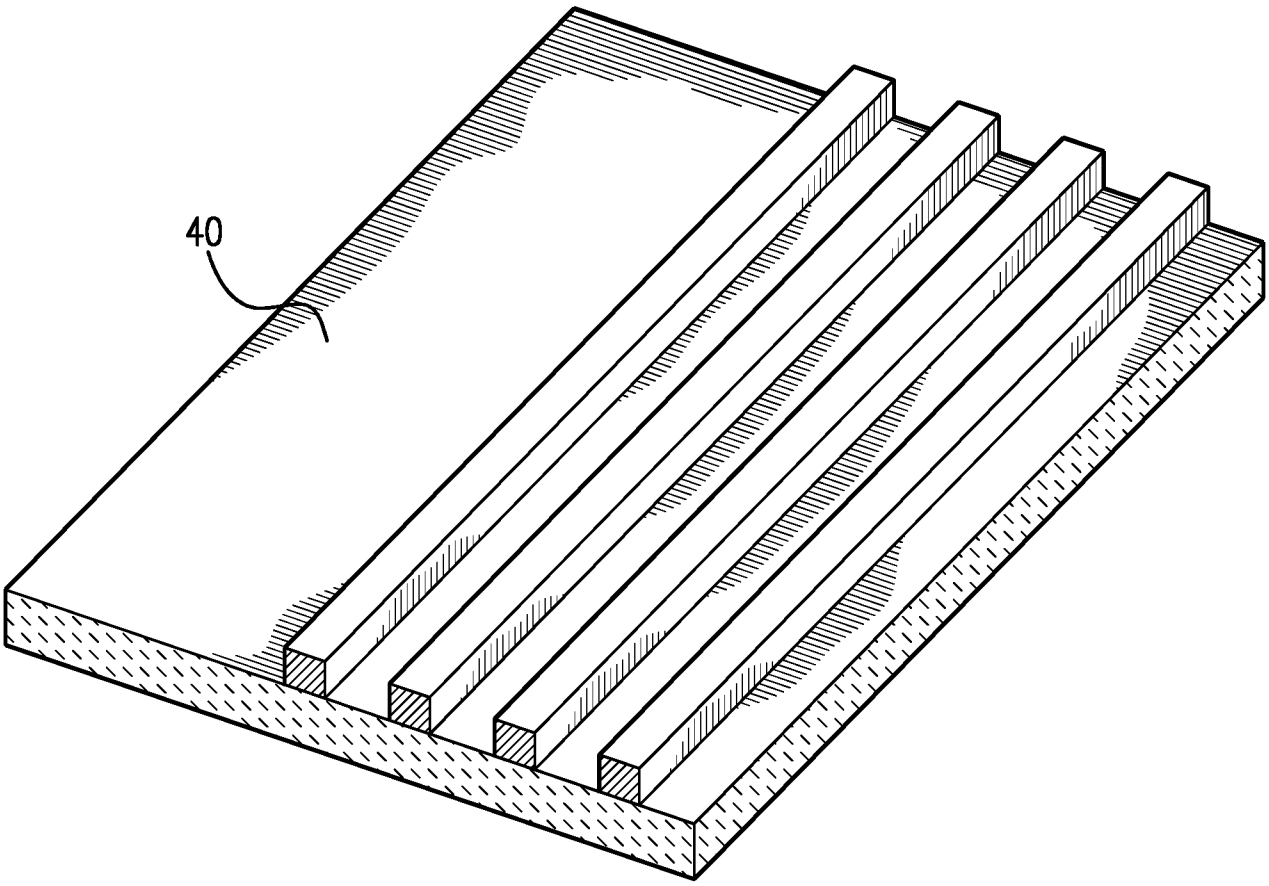

FIG. 9

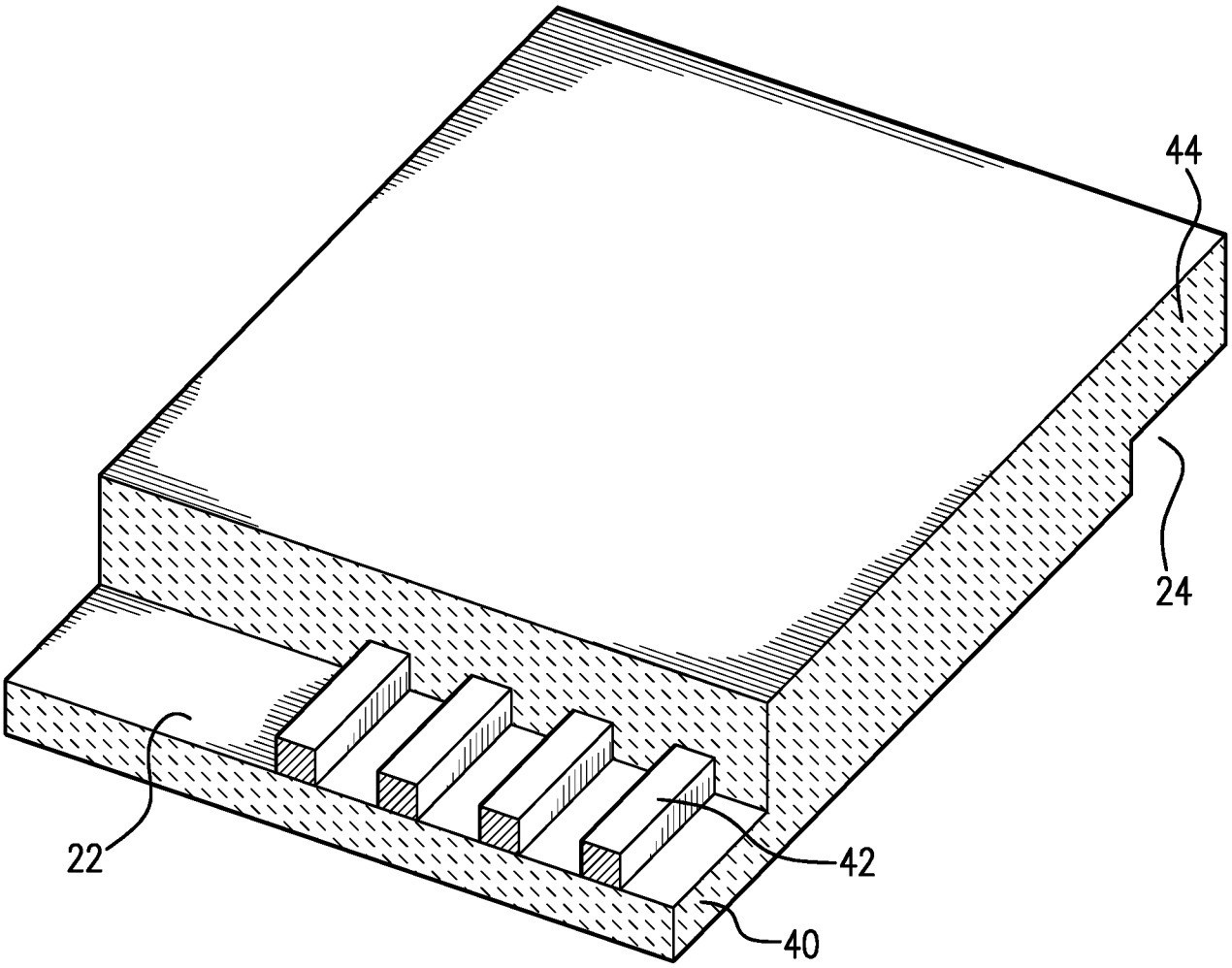

FIG. 10

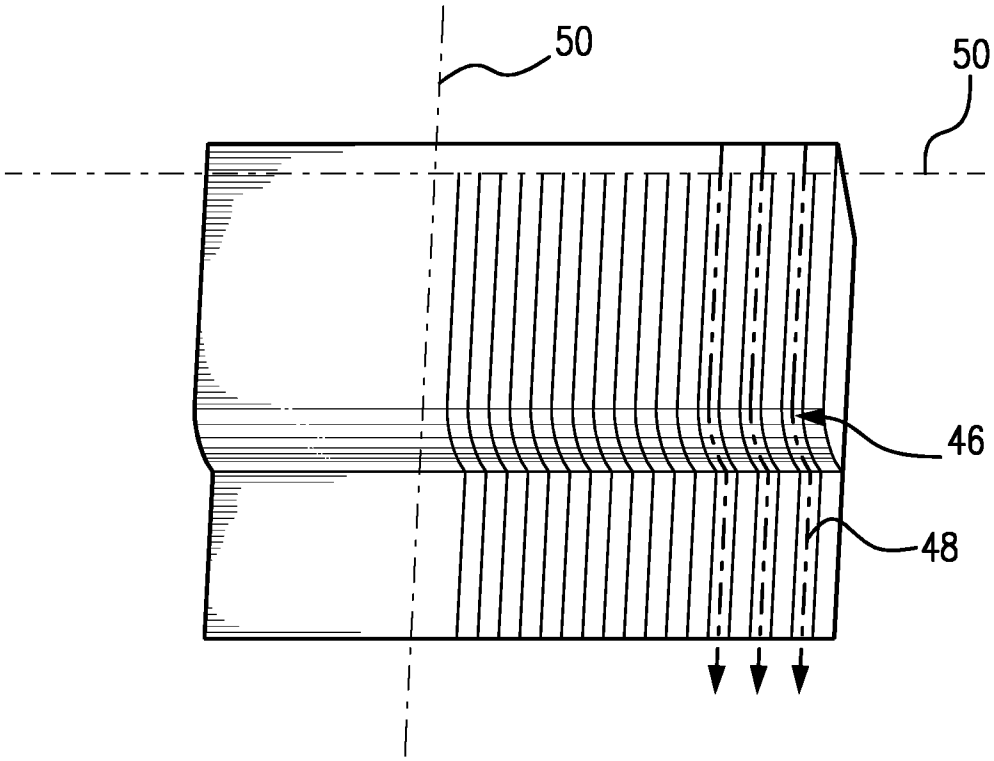

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/341 14

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05K 1/1 1, H05K 3/40 (2015.01)
CPC - H05K 1/1 1, H05K 3/40, H05K 3/403
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8)- H05K1/1 1, H05K3/40 (2015.01)
CPC- H05K1/1 1, H05K3/40, H05K3/403

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8)- H05K1/1 1, H05K3/40 (2015.01); CPC- H05K1/0277, H05K1/0278, H05K1/028, H05K1/1 1, H05K3/40, H05K3/403
USPC- 174/250,255; 361/749,750,751

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Proquest Dialog, Google Patents/Scholar,
Search terms used: electrical, interconnect, via, feedthrough, contact, non-planar, curved, bent, S-shaped, substrate, tape, ribbon, cable, ceramic, alumina, first, second, end, edge, expose, conductive, metal, strip, layer, laminate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y --- A	US 6,509,531 B2 (SAKAI et al.) 21 January 2003 (21.01.2003) Fig 1, abstract, col 7, ln 18-55	1-5, 8-12 ---------- 6, 7
Y --- A	US 5,028,473 A (VITIRIOL et al.) 02 July 1991 (02.07:1991) Fig 1c, 4, 5, abstract, col 3, ln 8-66, col 5, ln 51-63	1-5, 8-12 ---------- 6, 7

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"V later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being Obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 September 2015 (29.09.2015)	26 OCT 2015
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents- P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/341 14

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1 . **In order for all inventions to be examined, the appropriate additional examination fees must be paid.**

Group I: Claims 1-12 **drawn to an electrical interconnect.**

Group II: Claims 13-20 **drawn to a process for the manufacture of an electrical interconnect.**

see extra sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-12

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/341 14

Continuation of Box No. III - Observations where unity of invention is lacking

The inventions listed as Groups I through II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:
Group I includes the special technical feature of the ceramic substrate being non-planar, not included in the other group.

Group II includes the special technical feature of a plurality of electrically conductive strips being parallel to each other and electrically isolated from each other, shaping an assembly to a desired shape, and heating said assembly to a temperature and for a time effective to fuse said first green compact to said second green compact, not included in the other group.

Common Technical Features:
The only technical features shared by Groups I-II that would otherwise unify the groups, are that the electrical interconnect includes a ceramic material and includes portions of a conductive layer or strips that are exposed or not covered. However, these shared technical features do not represent a contribution over prior art, because the shared technical features are disclosed by US 6,509,531 B2 to Sakai et al. (hereinafter 'Sakai') 21 January 2003 (21.01.2003).

Sakai discloses an electrical interconnect structure including ceramic layers (22) and conductive layers (28) including exposed surfaces (25) (Fig 1, abstract, col 7, ln 15-55).

As the shared technical features were known in the art at the time of the invention, they cannot be considered special technical features that would otherwise unify the groups.

Therefore, Groups I-II lack unity under PCT Rule 13.

note: claim 14 is mistakenly written to depend from itself but is understood to depend from claim 13.